Novel Zero–Voltage and Zero–Current Switching Full-Bridge PWM Converter Using Simple Secondary Active Clamp Circuit

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Abstract —A novel zero-voltage and zero-current switching (ZVZCS) full-bridge phase shifted pulse-width modulation converter is presented in this paper. A simple auxiliary secondary circuit is used on the secondary side consist of capacitor, inductance, two rectifier diodes and unipolar MOSFET transistor, provides conditions for ZVZCS – soft switching of IGBT transistor on the primary side of the DC/DC converter. The turning off the MOSFET transistor located on the secondary side provides reset both secondary and primary current and thus the conditions for ZVZCS is achieved. This paper presents detail theoretical analysis and experimental results. The appropriateness of using the proposed new topology diagram for high power application is confirmed.

Keywords— phase-shifted PWM, power converter, insulated gate bipolar transistor, soft switching.

I. INTRODUCTION

Recently, the increasing demands for high performance load converters in power electronics are present. It also places great emphasis on increasing the switching frequency for reducing size and weight of the converters. However with increasing frequency the increasing switching losses occur mainly on the switching devices such as transistors. The power MOSFETs have many advantages such as very short switching times. It is one of the reasons why these switching devices are mainly used in ZCZVS FB PWM converters. However the MOSFETs are not suitable for high power applications. These days, IGBTs are replacing MOSFETs for high voltage, high power applications, since IGBTs have higher voltage rating, higher power density, and lower cost compared to MOSFETs [1]. On the other hand, the use of IGBTs is significantly reduced by their frequency switching, usually limited to 20 – 30 kHz because of their tail current characteristic [2]. To operate IGBTs at higher switching frequencies is required to significantly reduce turn – off switching losses. Many topologies have been developed to solve this problem [1] – [5]. This topology used auxiliary circuit on the secondary side to achieve ZCZVS and therefore to reduce the switching loss to zero. Generally the ZVS of the leading-leg switched is achieved by the similar manner as that of the ZVS FB PWM converters [3] – [4], [6] whereas ZCS of lagging-leg switches is achieved by resetting the primary current during the freewheeling period. The technical realization of auxiliary circuit which provides reset of primary current is realized in different ways. The converter proposed in [3] has simple auxiliary circuit which contains neither loss components nor active switches. Resetting of the primary current is achieved by using energy of leakage inductance and clamp capacitor placed on the secondary side. The converter [2] same as converter [3] contains neither loss components nor active switches. Resetting of the primary current is achieved using transformer auxiliary winding inserted into the secondary side what makes this auxiliary circuit more complex. The converter [7] contains active switch on the secondary side. This switch is used to control the clamping circuit. The clamp switch induces switching loss due to its hard switching, and the maximum output current is limited by the capacitance of holding capacitor [3]. The blocking capacitor on the primary side of the transformer winding is used in the converter [5]. The auxiliary circuit contains active switch and transformer auxiliary winding which make this circuit considerably complex and parameter design is complicated [2].

II. OPERATION PRINCIPLE

The detail description of proposed converter is in [6]. This operation principle description below is abbreviated form of description in [6].

The proposed converter (Fig.1) has nine operating modes within each operating half cycle. The equivalent circuits and the corresponding operation waveforms are show in Fig.2 and Fig.3, respectively.

Model- interval (t0–t1): The transistors T1, T2 are turned on with ZVS at t0 because only magnetizing current flows through diodes D1, D2. The collector current of the transistor T5, which is turned on at t0 too, starts to flow and the capacitor Cc is discharged.

The rise of the collector current is in resonant way with the resonant frequency \(\omega_{r1}\) different at no-load and short circuit in a range:

\[
\left(\frac{L_0 + L_{cs}}{C_0 C_c}, \frac{C_0 C_c}{C_0 + C_c}\right) \leq \omega_{r1} \leq \sqrt{\left(\frac{L_0 + L_{cs}}{C_c}\right) C_c} \tag{1}
\]
Mode2-interval (t1-t2): The transformer leakage inductance L_{LP} reflected to the primary side causes that primary current i_p is linearly increased with the slope U/L_{LP} while the secondary voltage u_s is zero as a result of commutation between output freewheeling diode D_0 and rectifier diode D_s.

Mode4-interval (t3-t4): Transistors T_1 and T_3 are conducting and the energy is delivered from the source to the load. The smoothing inductance current is a sum of the secondary current and inductance L_S current:

\[ i_o = i_s + i_{LS} \]  

Mode5-interval (t4-t6): The primary current increases with the slope:

\[ \frac{di_p}{dt} = \frac{U - nU_0}{L_{LP} + n^2L_0} + \frac{U}{L_m} \]  

Where \( n = \frac{N_P}{N_S} \) is power transformer turns ratio and \( L_m \) magnetizing inductance of the power transformer.

Mode6: interval (t6-t9): At t_6 the secondary transistor T_S turns off. At that time the commutation between transistor T_S and clamp diode D_C occurs and charging of the clamp capacitor C_C starts. Afterwards the commutation between D_C, D_3 and output freewheeling diode D_0 starts. In the mentioned commutation path the resonance occurs and rise of the current depends on the resonant frequency \( \omega_{R2} \):

\[ \omega_{R2} = \sqrt{\frac{(L_0 + L_{LS})C_0C_C}{C_0 + C_C}} \]  

for \( R_0 = \infty \).  

\[ \omega_{R2} = \sqrt{(L_0 + L_{LS})C_C} \]  

for \( R_0 = 0 \).  

During the commutation the energy stored in the leakage inductance is transferred to the clamp capacitor C_C and consequently an over-voltage \( \Delta U_3 \) appears on secondary voltage.

Mode7- interval (t6-t9): Only small magnetizing current \( i_m \) flows through primary winding of transformer. The output current flows trough output freewheeling diode D_0.

Mode8 - interval (t7-t8): In this interval the transistors T_1 and T_2 are turned off with ZCS. Only small magnetizing current \( i_m \) is switched off by transistors T_1 and T_2. The magnetizing current charges or discharges the internal output capacitances C_{OSS1} - C_{OSS4} of the IBGT transistors T_1 - T_4 respectively.

Mode9 - interval (t8-t9): At t_8 the freewheeling diodes D_1, D_4 starts to lead primary current and thus conditions for the ZVS for the transistors T_3 and T_4 are set up.

Fig.1. Circuit topology of the proposed converted

Fig.2. Equivalent circuit for each operation mode (Note—the blue color shows components among which commutations occur).
III. SIMULATION RESULTS

A simulation model in programme Orcad was created to verify the properties of the proposed converter. The simulations were made at input voltage $U = 325V$.

Parameters:
Transformer TR parameters:
- Turns ratio $n = 4$,
- Magnetizing inductance $L_m = 1 \text{ mH}$,
- Leakage inductance $L_{4P} = 5 \text{ µH}$.

Clamp circuit parameters:
- Clamp capacitor $C_c = 400 \text{ nF}$,
- Clamp inductance $L_S = 5 \text{ µH}$.

Fig. 4. shows the waveforms during turn-on and turn-off of the primary switch $T_4$. The influences of secondary active clamp circuit insure that all switching devices are switched softly. As we can see the leading-leg for transistor $T_4$ is switched softly and the switching loss is neglectable.

Fig. 5 shows the secondary voltage $u_{DS}$ and collector current $i_D$ of transistor $Ts$ (upper waveforms) in compare with switch waveforms of voltage $u_{CE}$ and collector current $i_C$ of transistor $T_4$ (bottom waveforms). It can be seen that influence of leakage inductance $L_{4S}$ of transformer and clamp inductance $L_S$ insure that turn-on of transistor $Ts$ is under zero-current and just as in the previous case (Fig.4) the power losses can be neglectable, too.

Fig. 6 and Fig. 7, respectively show simulation waveforms of voltage $u_{DS}$ and collector current $i_D$ of transistor $Ts$ (upper waveforms) in compare with primary voltage $u_P$ and current $i_P$ (bottom waveforms of Fig.6). After turned-off of secondary transistor $Ts$ only small magnetization current $i_m$ flows through the primary winding. This current charges and discharges the internal capacity of transistors $T_1$ – $T_4$, respectively and so the condition of ZVS is achieved. Fig.7. (bottom waveforms) shows the simulation waveforms of currents flows through clamp capacitor $C_c$, diode $D_s$ and clamp diode $D_c$ during cycle of operation $Ts$. 

Fig. 3. Operation waveforms of the proposed converter
IV. CONCLUSION

A novel zero-voltage and zero-current switching (ZVZCS) full bridge phase-shifted PWM converter is presented in this paper. The properties of the proposed converter topology were analyzed. Theoretical analysis was verified by simulation. It is shown that using of secondary active clamp circuit the soft switching conditions for all switching devices $T_1$ - $T_4$ located on the primary side is achieved.

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REFERENCES